



Seongjun Park

Jinseong Heo, Seongjun Jeong, Kiyoung Lee, Minhyun Lee, Seunggeol Nam, Yeonchoo Cho, Kyung-Eun Byun and Hyeon-Jin Shin

Device & System Research Center, Samsung Advanced Institute of Technology (SAIT), Republic of Korea

Two dimensional materials for electronic devices

Two dimensional (2D) materials including Graphene, h-BN, and Transition Metal Dichalcogenides (TMD's) have been studied intensively due to their exceptional electronic, optoelectronic, and mechanical properties. They have high electron mobility, high photo responsivity, and high flexibility. Thus, they have been considered as channel and component materials for post-Si technology.

A new device structure, Barristor, was proposed and demonstrated for 2D material devices. It is based on one of the unique properties of graphene, work function tenability. The key feature of the device is the modulation of barrier height between Graphene-semiconductor through the gate voltage modulation. The advantages of the new devices are high I_{on}/I_{off} ratio and compatibility of the process with current Si technology.

One of the key issues of the Barristor fabrications is Atomic Layer Deposition (ALD) for gate oxide. The effects of various surface modifications were systematically evaluated and compared. Then, equivalent of thickness close to the current Si technology was achieved and verified from an array of top-gated metal-oxide-graphene field-effect

transistors. Also, based on the new ALD technique, graphene heterojunction tunneling transistors were demonstrated with a low subthreshold swing value of < 60 mV/dec on an 8" glass wafer. Research on 2D material devices has been expanded into photodetector. Vertically stacked graphene heterojunctions have advantages of short transit length for photo-generated carriers and large sensing area. We demonstrated fast response time and high responsivity for graphene/TMD/graphene heterojunctions.

In addition, due to the chemical inertness and the atomically thin nature of 2D materials, they have been considered as interface materials in Si technology. For instance, graphene has been investigated for diffusion barrier for Cu interconnect. And, graphene was inserted between metal and Si to reduce the schottky barrier heights and contact resistance in source and drain, which is one of the most critical issues for scaling down. With the new concept of graphene insertion, low contact resistance was demonstrated.

In this presentation, we will cover the progresses in both 2D material devices and component materials in Si technology.